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*Property-Based System Design*

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### **Porting of IBM tools to support Accellera-standard version of PSL (Deliverable 3.3/2)**

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## Table of Revisions

Version	Date	Description and Reason	By	Affected Sections
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0.2	7.6.2005	Updated based on internal IBM review	A. Orni	All
0.3	29.6.2005	Updated based on review by PROSYD partners	A. Orni	All
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## Executive Summary

In the framework of the Prosyd project, each partner is committed to updating its tools to Accellera-standard PSL. IBM has undertaken this task in Deliverable 3.3/2, and this report describes the results that have been achieved.

PSL/Sugar originated as a proprietary language named "Sugar", which was used as the property specification language of the IBM tools, RuleBase PE and FoCs. As part of the Accellera effort for standardizing a property specification language, IBM proposed an enhanced version of the Sugar language, with the name Sugar 2.0. This proposal became the basis for the Accellera standard language, which is now called PSL.

At the starting point of the Prosyd project, the IBM tools supported a subset of Sugar 2.0. The supported subset only included the GDL flavour. Several language features were not supported, or were supported with restrictions. Some features whose definition had been modified or extended in the PSL standard, compared to their Sugar 2.0 definition, were supported in Sugar 2.0 style.

The goal of this deliverable was to upgrade the input language of the tools – RuleBase PE and FoCs – from the limited subset of Sugar 2.0 to PSL. This was done by adding support for new features, including entirely new support for the Verilog flavour, and by updating and expanding support for existing features, to bring them into compliance with the PSL standard. FoCs support was added for some features, which were previously supported only in RuleBase PE.

This document describes the current status of PSL support in the IBM tools, upon completion of Deliverable 3.3/2.

## Purpose

The purpose of this document is to describe the activity of porting IBM's RuleBase PE and FoCs verification tools to PSL, in the framework of Deliverable 3.3/2, and to present the achievements of this activity.

## Intended Audience

This document is intended for users of IBM's RuleBase PE and FoCs tools, and for tool vendors whose tools interact with RuleBase PE or FoCs. It is assumed that readers are familiar with the PSL language (as described in [3]).

## Background

The PSL/Sugar language has evolved hand-in-hand with the IBM verification tools, RuleBase PE and FoCs. It originated as a proprietary language named "Sugar", which was used as the property specification language of RuleBase PE and FoCs. In 2001, IBM joined the Accellera effort for defining a standard property specification language. As part of the standardization process, IBM proposed an enhanced version of the Sugar language, with the name Sugar 2.0 [1]. This proposal became the basis for the Accellera standard language, which is now called PSL. The standardization process required some modifications and additions to Sugar 2.0 until the final result, PSL, was achieved. The first version of PSL was version 1.0 [2], and the most recent version of the standard is PSL 1.1 [3].

As the PSL/Sugar language developed, it became necessary to port the RuleBase PE and FoCs tools to new versions of the language. The first step in this process was porting of the tools from the original Sugar language to Sugar 2.0. This porting stage was limited to a subset of Sugar 2.0, which consisted mainly of features that were analogous to Sugar features. It included only the GDL flavour, and did not extend support to the new flavours defined in Sugar 2.0.

In the period following this initial step, a small set of additional features was implemented and added to the supported subset.

Thus, at the starting point of the Prosyd project, the IBM tools supported a subset of Sugar 2.0. This subset was limited in several respects: in features that were not supported, in features that were supported in Sugar 2.0 style, but had been redefined or extended in the PSL standard, and in features whose support was incomplete.

In the framework of the Prosyd project, each partner is committed to updating its tools to Accellera-standard PSL. IBM has undertaken this task in Deliverable 3.3/2, and this report describes the results that have been achieved.

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# Glossary

## **Accellera**

The mission of the Accellera organization is to drive worldwide development and use of standards required by systems, semiconductor and design tools companies, which enhance a language-based design automation process.

## **GDL**

GDL (General Description Language) is the modeling language of the IBM verification tools, RuleBase PE and FoCs. Its primary purpose is to describe the environment for formal verification. However, it is also used in conjunction with PSL to aid specification of a design.

## **FoCs**

FoCs is the IBM checker generation tool, developed by the IBM Haifa Research Laboratory. FoCs takes PSL properties and translates them into HDL Checkers, which in turn are integrated into the simulation environment.

## **PSL**

Property Specification Language, the language for specification of designs upon which PROSYD is based.

## **RuleBase PE**

RuleBase Parallel Edition (PE) is an industrial-strength formal verification tool, developed by the IBM Haifa Research Laboratory. RuleBase PE is especially applicable for verifying the control logic of large hardware designs.

## **Sugar**

The language originally used by IBM's RuleBase PE and FoCs tools as a property specification language, which served as the basis for Sugar 2.0 and PSL.

## **Sugar 2.0**

The language proposed by IBM, which served as the basis for the Accellera PSL standard.

## **Verilog HDL**

One of two standardized hardware description languages used to specify the structure and behaviour of electronic systems in textual format. Developed in the mid-1980s as a proprietary language and acquired by Cadence Design Systems, it became a de facto industry standard. In the mid-90s Cadence placed it into the public domain and it became a de jure standard promulgated by the Institute of Electric and Electronic Engineers (IEEE). Verilog is also the name of a legacy simulation tool offered by Cadence.

# 1 Introduction

When work on this deliverable began, in January 2004, the IBM tools supported a subset of Sugar 2.0, which was mainly characterized by its strong correlation to the original Sugar language. The supported subset only included the GDL flavour. Several language features which were defined in Sugar 2.0 (and subsequently in PSL), but had not existed in Sugar, were not supported, or were supported with restrictions. Some features whose definition had been modified or extended in the PSL standard, compared to their Sugar 2.0 definition, were supported in Sugar 2.0 style.

The goal of this deliverable was to upgrade the input language of the tools – RuleBase PE and FoCs – from the limited subset of Sugar 2.0 to PSL. This was done by adding support for new features, including entirely new support for the Verilog flavour, and by updating and expanding support for existing features, to bring them into compliance with the PSL standard. The results of this activity are described in 2.

The language currently supported by RuleBase PE and FoCs is a subset of PSL, and still does not encompass the entire PSL definition. The PSL language includes a very large set of features, and each of the PSL-supporting tools that exist today has started by supporting a limited subset, which is continually extended as the demand for PSL support grows. The subset of PSL that is now supported by the IBM tools, following the porting effort, is improved both in its extent and in its conformance with the standard. This places the IBM tools in a good position for interoperability with other PSL-supporting tools.

# 2 Current PSL Support in IBM Tools

This section describes the status of PSL support in the IBM tools, RuleBase PE and FoCs, upon completion of Deliverable 3.3/2 on July 1, 2005.

Note that all constructs are supported within the restrictions of the PSL Simple Subset, as defined in PSL LRM 1.1, section 4.4.4 (except for OBE operators, which are supported without restrictions).

## Flavours

RuleBase PE and FoCs support two flavours: GDL and Verilog.

## Boolean Layer

- GDL or Verilog expressions (according to the flavour)
- The logical operators `->` and `<->`
- The **union** operator
- The builtin functions **rose()**, **fell()**, **prev()**, **next()**

## Temporal Layer

- FL operators **always**, **G**, **next**, **X**, **next[i]**, **next\_a**, **next\_e**, **next\_event**, **next\_event\_a**, **next\_event\_e**, **until**, **until\_**, **W**, **before**, **before\_**
- FL strong operators **eventually!**, **F**, **until!**, **until!\_**, **U**, **before!**, **before!\_**, **next\_event!** (RuleBase PE only)
- All SERE and sequence operators
- Suffix implication:  $\{SERE\} \rightarrow \{SERE\}$ ,  $\{SERE\} \Rightarrow \{SERE\}$ , and  $\{SERE\}(f)$ , either at the top level of a property or nested inside a top-level **always**
- The **never** operator, applied to sequences or boolean expressions
- Replicated properties using the **forall** operator (RuleBase PE all flavours, FoCs GDL flavour only)
- Clocked properties using the **@** operator, applied at the top level of a property
- The **abort** operator, applied at the top level of a property
- Named properties, sequences, and endpoints, including parameters
- All OBE operators

## Verification Layer

- Verification directives **assert**, **cover**, **restrict** (**cover** is supported in FoCs, and in RuleBase PE with FormalSim; **restrict** is supported in RuleBase PE only)

- The **assume** verification directive (RuleBase PE only), applied to safety properties of the simple subset (except for the  $\rightarrow$  and  $\Rightarrow$  operators)
- Verification units of type **vunit**, **vmode**, **vprop**
- Verification unit inheritance
- Default clock declarations
- Report strings (FoCs only)

### **Modeling layer**

- In GDL flavour, all of the GDL language is supported
- In Verilog flavour, the synthesizable subset of Verilog is supported (IEEE 1364.1-2002 annex A), except for the following constructs: library, configuration, localparam, genvar, PATHPULSE\$, generated instantiation, attributes
- Structures are not supported

# 3 References

- [1] Sugar 2.0 proposal presented to the Accellera Formal Verification Technical Committee, March 20 2002.  
[http://www.haifa.il.ibm.com/projects/verification/sugar/Sugar\\_2.0\\_Accellera.ps](http://www.haifa.il.ibm.com/projects/verification/sugar/Sugar_2.0_Accellera.ps)
- [2] Accellera, Property Specification Language v.1.0, October 4 2003.  
[http://www.eda.org/vfv/docs/psl\\_1rm-1.0.pdf](http://www.eda.org/vfv/docs/psl_1rm-1.0.pdf)
- [3] Accellera, Property Specification Language v.1.1, April 2004.  
<http://www.eda.org/vfv/docs/PSL-v1.1.pdf>